Applied Physics Express 7, 041003 (2014)
http://dx.doi.org/10.7567/APEX.7.041003

Normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT on 8 in. Si with Low Leakage Current and High Breakdown Voltage (825 V)

Joseph J. Freedsman[1]*, Takashi Egawa[1], Yuya Yamaoka[2], Yoshiki Yano[2], Akinori Ubukata[2], Toshiya Tabuchi[2], and Koh Matsumoto[3]

[1]*Research Center for Nano-Device and System, Nagoya Institute of Technology, Nagoya 466-8555, Japan*
[2]*Taiyo Nippon Sanso Corporation, Tsukuba, Ibaraki 300-2611, Japan*
[3]*Taiyo Nippon Sanso EMC Ltd., Tama, Tokyo 206-0001, Japan*
E-mail: freedy54@gmail.com

Received January 21, 2014; accepted March 13, 2014; published online April 2, 2014

We report recessed-gate Al_2O_3/AlGaN/GaN normally-OFF metal–oxide–semiconductor high-electron-mobility transistors (MOS-HEMTs) on 8 in. Si. The MOS-HEMTs showed a maximum drain current of 300 mA/mm with a high threshold voltage of +2.4 V. The quite low subthreshold leakage current ($\sim 10^{-8}$ mA/mm) yielded an excellent ON/OFF current ratio (9×10^8) with a small, stable subthreshold slope of 74 mV/dec. An atomic-layer-deposited Al_2O_3 layer effectively passivates, as no significant drain current dispersions were observed. A high OFF-state breakdown voltage of 825 V was achieved for a device with a gate-to-drain distance of 20 μm at a gate bias of 0 V.

AlGaN/GaN high-electron-mobility transistors (HEMTs) on Si substrates have emerged as promising candidates for high-power applications owing to improved GaN epitaxial growth and large-size scalability of low-cost Si.[1,2] These HEMTs show normally-ON operation because of the existence of a two-dimensional electron gas (2DEG) produced by spontaneous and piezoelectric polarization in AlGaN/GaN heterostructures. However, high-speed and high-efficiency power switching applications require normally-OFF GaN devices on large Si substrates to accommodate large-scale monolithic integration.[3–5] In addition, a normally-OFF device with a high positive threshold voltage V_{th}, large gate voltage swing (GVS), and low leakage current as well as high blocking capabilities would deliver circuit design simplicity, safety, and reliability. For high-power device applications, all these criteria should be achieved simultaneously on a large Si platform.

Various technologies for fabricating normally-OFF GaN devices have been demonstrated, such as fluorine plasma treatment,[5] recessed-gate AlGaN/GaN HEMTs,[6] gate injection transistors,[7] tunnel-junction field-effect transistors,[8] and dual-gate AlGaN/GaN transistors.[9] The problem with recessed AlGaN/GaN Schottky gate transistors is their small positive V_{th} (typically $\leq$2 V) with high gate leakage I_g, which can degrade the switching performance and limit the forward GVS.[10] To enhance the forward gate voltage and reduce I_g, AlGaN/GaN recessed-gate metal–oxide–semiconductor (MOS) HEMTs were used.[10–14] However, some recessed MOS-HEMTs also suffered from low positive V_{th} and high forward I_g.[12,13] An AlGaN/GaN MOS-HEMT with a high positive V_{th} (>+2 V) and low I_g was demonstrated recently on 4 in. Si by using SiN_x and SiO_2 as gate dielectrics.[3,14] Compared with these dielectrics, an Al_2O_3 layer fabricated by atomic layer deposition (ALD) offers the advantages of high uniformity, scalability, and low defect density in combination with its large band gap (~7 eV), high dielectric constant (~9), and high breakdown field strength ($\geq$10 MV/cm).[15] To date, there is no report of Al_2O_3/AlGaN/GaN normally-OFF MOS-HEMTs on a large (8 in.) Si platform.

In this letter, we demonstrate a recessed-gate Al_2O_3/AlGaN/GaN normally-OFF MOS-HEMT with reduced OFF-state leakage currents, lower current collapse, and high blocking voltages achieved simultaneously on an 8 in. Si substrate. The fabricated normally-OFF devices showed a high positive V_{th} of +2.4 V with low off-state leakage currents (I_d, I_g, $\sim 10^{-8}$ mA/mm). A high I_{on}/I_{off} ratio of 9×10^8 and small, stable subthreshold swing (SS) of 74 mV/dec were observed as a result of the low leakage. Further, the normally-OFF device with a gate-to-drain distance L_{gd} of 20 μm showed a high breakdown voltage of 825 V at a gate bias (V_g) of 0 V. The results of this work on GaN normally-OFF devices on 8 in. Si are compared with the state-of-the-art normally-OFF GaN power devices reported on smaller Si substates ($\leq$4 in.).

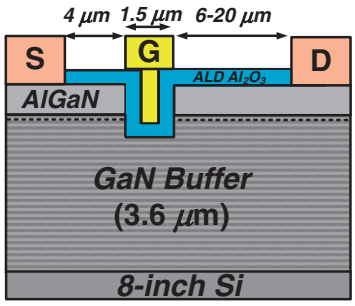

Fig. 1. Schematic cross-sectional view of as-fabricated recessed-gate normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT on 8 in. Si.

The AlGaN/GaN heterostructure was grown on an 8 in., Si(111) substrate using a Taiyo Nippon Sanso UR26 K multi-wafer (6×8 in.) metalorganic chemical vapor deposition reactor. The heterostructure consists of a 1 nm GaN cap, 25 nm AlGaN barrier, 1 nm AlN spacer, 0.5 μm GaN channel, and 2.4 μm buffer and transition layers. A schematic cross-sectional view of the as-fabricated recessed-gate Al_2O_3/AlGaN/GaN MOS-HEMT on 8″ Si is shown in Fig. 1. The heterostructure consists of a 1 nm GaN cap, 32 nm $Al_{0.23}Ga_{0.77}N$ barrier, 1 nm AlN spacer, and 3.6 μm GaN buffer and transition layers. Wafer mapping and room temperature Hall effect measurements across the wafer in the horizontal and vertical directions along the diameter yielded uniformly high mobility and sheet carrier concentration values of 1520 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 1.13×10^{13} cm^{-2}, respectively. These results are comparable with the recently reported values for an AlGaN/GaN heterostructure on 8 in. Si.[16]

The MOS-HEMT fabrication started with mesa isolation using BCl_3-plasma-based reactive ion etching (RIE). The source/drain ohmic contacts were formed by e-beam evaporation of a Ti/Al/Ni/Au (15/72/12/40 nm) metal stack and subsequent rapid thermal annealing (RTA) at 850 °C for 30 s. To obtain a high positive V_{th} (>0 V), a gate mask was used to etch about 40 nm by RIE at low power with a slow etching rate. The gate footprint defined by etching was 1.5 μm for devices with a gate-to-drain distance of $L_{gd} \sim 4$ to 20 μm. The samples were cleaned with buffered hydrofluoric acid solution followed by ALD of a 20 nm Al_2O_3 layer using trimethylaluminum, ozone, and water vapor as precursors. Post-deposition annealing of the Al_2O_3 layer was conducted at 600 °C by RTA in N_2 ambient. The gate metals (Pd/Ti/Au: 40/20/80 nm) were deposited on the Al_2O_3 layer. Finally, the oxide layer in the ohmic contacts was etched by a buffer-based oxide etchant. The MOS-HEMTs DC and pulsed I_{ds}–V_{ds} and characteristics were measured using an Agilent B1500A semiconductor device analyzer. The OFF-state leakage and three-terminal breakdown voltage (BV) characteristics were measured using a Keithley pico-ammeter interfaced with a probe station and a computer. For the BV measurements, a V_g of 0 V was applied, and the Si substrate was grounded.

Figure 2(a) shows the semi-log scale transfer characteristics of a recessed-gate Al_2O_3/AlGaN/GaN normally-OFF MOS-HEMT. The subthreshold leakage current (I_d, I_g) levels in the MOS-HEMT were on the order of $\sim 10^{-8}$ mA/mm. This value is roughly several orders of magnitude lower than that of a Schottky-gate HEMT on 8 in. Si[16] or Al_2O_3/AlGaN/GaN normally-OFF MOS-HEMTs on sapphire.[17,18] Thus, a 40-nm-deep recess created a barrier in the conduction band sufficient to obstruct the electrons, and thus ensures complete normally-OFF operation with a low I_d of 10^{-8} mA/mm at $V_{gs} = +2.4$ V and $V_{ds} = 8$ V. To evaluate the surface leakage current (I_{surf}), measurements were made up to 100 V between two adjacent ohmic mesas separated by 10 μm and passivated with an $A1_2O_3$ layer. The $A1_2O_3$ layer effectively mitigated I_{surf}, as it remained low, on the order of 10^{-8} mA/mm. A substantially lower leakage current also showed excellent subthreshold characteristics such as a high I_{on}/I_{off} ratio of 9×10^8 with a stable, small SS value ($SS = \partial V_{gs}/\partial \log I_{ds}$) of 74 mV/dec.

A peak transconductance (g_{mmax}) of 79 mS/mm was observed from the transfer characteristics. By definition,[19] V_{th} was extracted as +2.4 V from the $\sqrt{I_{ds}}$ versus V_{gs} plot. The statistical calculations of the measured devices yielded an average threshold voltage of +2.36 V with a standard deviation of $\sigma_{Vth} = 0.11$ V. This indicates a high degree of uniformity and conformality in the recess and subsequent ALD processes, respectively. As shown in Fig. 2(b), the normally-OFF MOS-HEMT exhibited a tiny V_{th} hysteresis of 0.1 V with no changes in I_{dsmax} for a shuttle gate bias sweep from −6 to + 9 V. Further, a lower V_{th} hysteresis and forward I_g enabled a high drain current drivability and a large gate overdrive of +9 V, respectively, for the recessed-gate MOS-HEMT, which is better than the reported values for Al_2O_3/AlGaN/GaN-based normally-OFF MOS-HEMTs.[13,17,18]

Figure 3(a) shows the DC I_{ds}–V_{ds} characteristics of the Al_2O_3/AlGaN/GaN normally-OFF MOS-HEMT. The MOS-HEMT showed a high drain current density I_{dsmax} of 300 mA/mm with a specific ON-resistance $R_{on,sp}$ of 2.5 mΩ·cm^2. The I_{dsmax} value was low owing to partial depletion of the 2-DEG under the gate region. Pulsed I_{ds}–V_{ds} measurements were conducted with a pulse width and period of 500 μs and 10 ms, respectively. A quiescent gate and drain bias condition of $V_{ds\text{-}q} = 40$ V, $V_{gs\text{-}q} = 0$ V was applied. The pulsed drain current was compared with the reference gate and drain bias conditions of $V_{gs\text{-}0} = V_{ds\text{-}0} = 0$ V. As shown in Fig. 3(b), under the pulsing criterion, the drain current dispersions were low up to $V_{ds} = 40$ V and at $V_{gs} = +9$ V. The results also indicate that the fabricated normally-OFF MOS-HEMT has a good oxide/semiconductor interface, which is supported by the observations of a low V_{th} hysteresis even during operation at a high forward gate bias,[13] as well as the stable and small SS value.[20]

Figure 4(a) shows the OFF-state leakage and breakdown characteristics evaluated for a normally-OFF MOS-HEMT with $L_{gd} = 20$ μm. The BV criterion is defined as the drain voltage V_{ds} at which a drain current I_d of 1 mA/mm was observed. The BV characteristics reveal that the source injection and gate leakage currents were low (~μA/mm) up to 800 V. The low source injection current was due to our highly resistive buffer, which serves as a current blocking layer between the ohmic electrodes,[1] and I_g was minimized by using atomic-layer-deposited Al_2O_3 as the gate dielectric. The substrate leakage current I_{sub} dominates as V_{ds} is increased beyond 500 V and triggers drain breakdown at 825 V. Similar observations of increased I_{sub} were also reported for other normally-OFF GaN devices on Si substrates.[5,9]

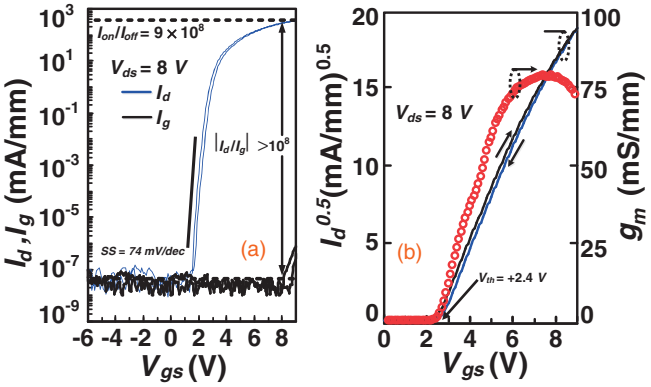

Fig. 2. (a) Semi-log scale transfer (I_d–V_{gs}, I_g–V_{gs}) characteristics and (b) transfer characteristics of recessed-gate normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT on 8 in. Si with bidirectional gate voltage sweep, $W_g/L_g = 15/1.5$ μm.

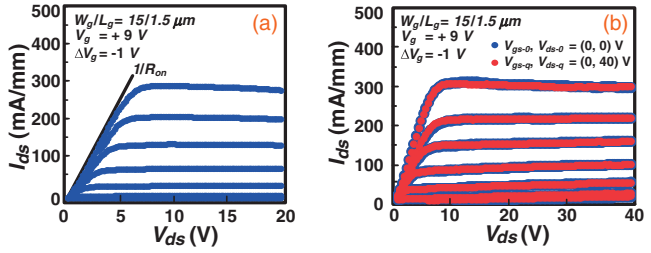

Fig. 3. (a) DC I_{ds}–V_{ds} characteristics and (b) pulsed I_{ds}–V_{ds} characteristics of normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT on 8 in. Si. A 500 μs pulse width and 10-pulse period were used.

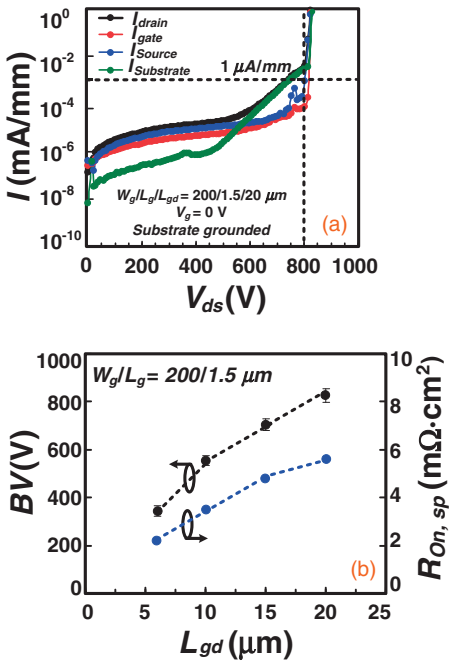

Fig. 4. (a) Three-terminal OFF-state leakage/breakdown characteristics of normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT with $L_{gd} = 20\,\mu m$ and (b) BV and specific ON-resistance versus L_{gd} of normally-OFF MOS-HEMTs on 8 in. Si.

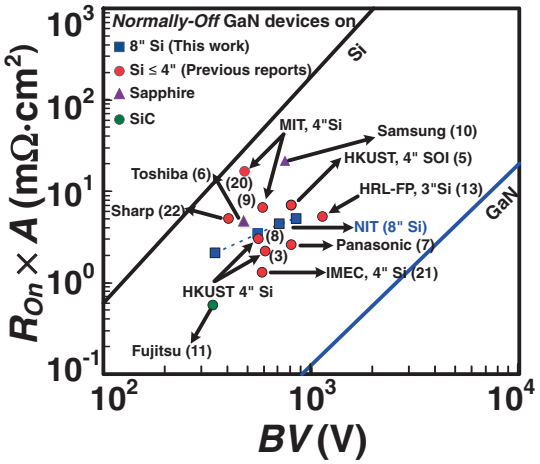

Fig. 5. Specific ON-resistances and breakdown voltages of GaN-based normally-OFF power devices on 8 in. Si compared with those in previous reports. Si substrate diameter sizes are indicated.

Figure 4(b) shows the specific ON-resistance ($R_{on,sp}$) and BV measured at $V_g = 0\,V$ for normally-OFF MOS-HEMTs with varying L_{gd}. The $R_{on,sp}$ values were calculated from the linear region of I_{ds}–V_{ds} at $V_g = 9\,V$ and $V_{ds} = 1.5\,V$, with the active device area including the channel and 2-μm transfer length from the source and drain contacts.[20] Figure 5 shows the $R_{on,sp}$ and breakdown characteristics of normally-OFF GaN devices on smaller Si substates (≤4 in.)[21,22] compared with those of the Al_2O_3/AlGaN/GaN MOS-HEMTs on 8″ Si in this work. The comparison clearly shows that the GaN normally-OFF device on 8″ Si exhibits good BV characteristics due to low OFF-state leakage currents without using Si on insulator (SOI)[5] or field plate (FP) technologies.[13] This demonstrates the process compatibility of GaN normally-OFF high-power MOS devices on a large (≥8 in.) Si substrate.

Normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMTs with a low leakage current and high breakdown voltage on an 8 in. Si substrate were demonstrated. The MOS-HEMTs showed a high positive threshold voltage of +2.4 V with a very low off-state leakage current (~10^{-8} mA/mm). An I_{dmax} of 300 mA/mm and $R_{on,sp}$ of 2.5 mΩ·cm² was observed at a high input gate bias of +9 V. A high I_{on}/I_{off} ratio of 9×10^8 accompanied a small, stable SS of 74 mV/dec for this device. The normally-OFF MOS-HEMTs showed no significant drain current dispersions owing to effective passivation by an atomic-layer-deposited Al_2O_3 layer. A high BV of 825 V and low leakage currents were observed for the normally-OFF device with an L_{gd} of 20 μm, which is also the highest BV reported for normally-OFF GaN devices on 8 in. Si.

Acknowledgment J. J. Freedsman duly thanks the Venture Business Laboratories, Nagoya Institute of Technology for a post-doctoral fellowship.

1) T. Egawa, IEDM Tech. Dig., 2012, p. 613.
2) J. J. Freedsman, T. Kubo, and T. Egawa, Appl. Phys. Lett. **101**, 013506 (2012).
3) Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang, and K. J. Chen, IEEE Electron Device Lett. **34**, 1373 (2013).
4) W. Chen, K.-Y. Wong, and K. J. Chen, IEEE Electron Device Lett. **30**, 430 (2009).
5) Q. Jiang, C. Liu, Y. Lu, and K. J. Chen, IEEE Electron Device Lett. **34**, 357 (2013).
6) W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, IEEE Trans. Electron Devices **53**, 356 (2006).
7) Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, IEEE Trans. Electron Devices **54**, 3393 (2007).
8) H. Chen, L. Yuan, Q. Zhou, C. Zhou, and K. J. Chen, Phys. Status Solidi C **9**, 871 (2012).
9) B. Lu, O. I. Saadat, and T. Palacios, IEEE Electron Device Lett. **31**, 990 (2010).
10) K. Kim, S. Jung, D. Kim, H.-S. Kang, K.-S. Im, J.-J. Oh, J.-B. Ha, J.-K. Shin, and J.-H. Lee, IEEE Electron Device Lett. **32**, 1376 (2011).
11) M. Kanamura, T. Ohki, T. Kikakawa, K. Imanishi, T. Imada, A. Yamada, and N. Hara, IEEE Electron Device Lett. **31**, 189 (2010).
12) K. S. Boutros, S. Burnham, D. Wong, K. Shinohara, B. Hughes, D. Zehnder, and C. McGuire, IEDM Tech. Dig., 2009, p. 161.
13) R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, IEEE Electron Device Lett. **32**, 632 (2011).
14) B.-R. Park, J. Lee, W. Choi, H. Kim, K.-S. Seo, and H.-Y. Cha, IEEE Electron Device Lett. **34**, 354 (2013).
15) Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, V. Sahmuganathan, T. Xu, and C. H. Lee, IEEE Electron Device Lett. **31**, 96 (2010).
16) D. Christy, T. Egawa, Y. Yano, H. Tokunaga, H. Shimamura, Y. Yamaoka, A. Ubukata, T. Tabuchi, and K. Matsumoto, Appl. Phys. Express **6**, 026501 (2013).
17) Z. Xu, J. Wang, Y. Liu, J. Cai, J. Liu, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, and J. Zhang, IEEE Electron Device Lett. **34**, 855 (2013).
18) Y. Wang, M. Wang, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen, and B. Shen, IEEE Electron Device Lett. **34**, 1370 (2013).
19) S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981) 2nd ed., p. 324.
20) B. Lu, E. Matioli, and T. Palacios, IEEE Electron Device Lett. **33**, 360 (2012).
21) F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain, and G. Borghs, IEEE Electron Device Lett. **31**, 111 (2010).
22) T. Oka and T. Nozawa, IEEE Electron Device Lett. **29**, 668 (2008).