Reprinted from

APPLIED PHYSICS EXPRESS

Uniform Growth of AlGaN/GaN High Electron Mobility Transistors on 200 mm Silicon (111) Substrate

Dennis Christy, Takashi Egawa, Yoshiki Yano, Hiroki Tokunaga, Hayato Shimamura, Yuya Yamaoka, Akinori Ubukata, Toshiya Tabuchi, and Koh Matsumoto

Appl. Phys. Express **6** (2013) 026501

Applied Physics Express 6 (2013) 026501
http://dx.doi.org/10.7567/APEX.6.026501

Uniform Growth of AlGaN/GaN High Electron Mobility Transistors on 200 mm Silicon (111) Substrate

Dennis Christy[1]*, Takashi Egawa[1], Yoshiki Yano[2], Hiroki Tokunaga[2], Hayato Shimamura[3], Yuya Yamaoka[2], Akinori Ubukata[2], Toshiya Tabuchi[2], and Koh Matsumoto[3]

[1]*Research Center for Nano-Device and System, Nagoya Institute of Technology, Nagoya 466-8555, Japan*
[2]*Taiyo Nippon Sanso Corporation, Tsukuba, Ibaraki 300-2611, Japan*
[3]*Taiyo Nippon Sanso EMC Ltd., Tama, Tokyo 206-0001, Japan*
E-mail: dennischristy82@yahoo.co.in

Received October 16, 2012; accepted December 20, 2012; published online January 21, 2013

Crack-free AlGaN/GaN high-electron-mobility transistors (HEMTs) grown on a 200 mm Si substrate by metal–organic chemical vapor deposition (MOCVD) is presented. As grown epitaxial layers show good surface uniformity throughout the wafer. The AlGaN/GaN HEMT with the gate length of 1.5 μm exhibits a high drain current density of 856 mA/mm and a transconductance of 153 mS/mm. The 3.8-μm-thick device demonstrates a high breakdown voltage of 1.1 kV and a low specific on-resistance of 2.3 mΩ cm^2 for the gate–drain spacing of 20 μm. The figure of merit of our device is calculated as 5.3 × 10^8 V^2 Ω^{-1} cm^{-2}. © 2013 The Japan Society of Applied Physics

In recent years, AlGaN/GaN high-electron-mobility transistors (HEMTs) have been proven to be the ideal choice of materials for next-generation high-power device application due to their excellent material properties. The demand for low-cost production of GaN-based devices for high-power, high-frequency, and high-temperature operations has propelled the development of a variety of substrates like sapphire, SiC, and Si.[1–7] Among them, the Si substrate offers the benefits of low cost and the availability of large-area substrate, which reduce the cost of the device processing.[8] For power device application, the Si substrate has become a very attractive alternative to sapphire and SiC for substrate diameters larger than 150 mm. Recently, GaN device fabrication on a 200 mm Si(111) substrate has become a challenging task for the electron devices community due to the huge market potential.

Only limited success has been achieved in developing high-quality single and double heterostructures of AlGaN/GaN on a 200 mm Si wafer due to the issues like epilayer cracking, wafer bowing, and high density of point and line defects.[9–11] The main challenges in growing GaN epitaxy on Si originate from wafer bowing due to the strain from the lattice mismatch of the heteroepitaxy, the thermal expansion coefficient of GaN epitaxy relative to Si, and the temperature gradient through the wafer from outside heating.

Although the lattice and thermal mismatches of GaN on Si generate dislocations and epilayer cracks, AlGaN/GaN HEMTs have shown attractive device performance for high-power applications.[12–14] For example, a high-power device figure of merit (FOM) of 2.6 × 10^8 V^2 Ω^{-1} cm^{-2} obtained by Selvaraj et al. and a high breakdown voltage of more than 1.5 kV demonstrated for AlGaN/GaN on 100 mm Si by Lu and Palacios using substrate removing technology were reported.[15,16] But only few reports are available in the literature on the growth of crack-free, uniform, high-crystalline quality AlGaN/GaN heterostructure epitaxial layers on 200 mm Si for practical device applications.

In this letter, we report the high quality and uniform AlGaN/GaN epilayers grown on a 200 mm Si(111) substrate carried out in a 6 × 8 in. multiwafer (Taiyo Nippon Sanso UR26K) metal–organic chemical vapor deposition (MOCVD) reactor, and subsequently, the fabrication and excellent device characteristics of HEMTs. A high-temperature AlN nucleation layer of thickness about 130 nm, often used to avoid the diffusion of Ga into the Si substrate, was grown followed by 250-nm-thick $Al_{0.3}Ga_{0.7}N$ layers. The buffer layer in the device structure that consists of 80 strained layer superlattice (SLS) pairs yielded a total buffer thickness of 2.4 μm used to control strain balance on the large-area wafer. An unintentionally doped GaN (UID-GaN) layer of 1-μm-thick was grown over the buffer layer. The epilayers including buffer layers and an active AlGaN layer of 25-nm-thick were grown at a high-temperature of 1130 °C. A 1-nm-thick AlN spacer was deposited over GaN to improve the two-dimensional electron gas (2DEG) mobility in the channel.

The device processing steps were followed according to our previous work in Ref. 12. Mesa isolation of devices was done using BCl_3 plasma with reactive ion etching for 30 min. The dielectric passivation of devices was done with 100-nm-thick SiO_2. The metallization scheme for ohmic contacts is Ti/Al/Ni/Au (15/72/12/40 nm) followed by lift-off and rapid thermal annealing at 850 °C for 30 s in N_2 atmosphere. The Schottky gate metals (Pd/Ti/Au = 40/20/60 nm) were deposited by electron beam evaporator. No further post passivation was performed in our devices. The Hall measurement by the Van der Pauw method was carried out to characterize the 2DEG. Indium was used as the ohmic contact for room-temperature Hall measurement, while Ti/Al alloy was used for Hall mobility and sheet carrier concentration measurements with varying temperatures. The three-terminal off-state breakdown voltage (3TBV) was measured between the source and drain ohmic contacts for different gate–drain spacings (L_{gd} = 6 to 20 μm). The test devices are gate biased at −6 V with the Si substrate grounded.

Figure 1(a) shows that the image of as-grown AlGaN/GaN heterostructure, which is a clear evidence for the growth of heterostructure epilayers free of cracks from the center to the edges of the wafer. Figures 1(b) and 1(c) further confirm the uniformity of epitaxial layers in terms of average film thickness of 3.71 μm with the standard deviation of 0.053 μm and the average Al composition of 23.1% with a standard deviation of 0.71% carried out using white light interference and photoluminescence, respectively. Thus, the uniformity of epitaxial layers was effectively controlled over wide area of the wafer at higher growth temperature. The uniformity of our grown heterostructure on the 200 mm Si wafer as seen from the images is

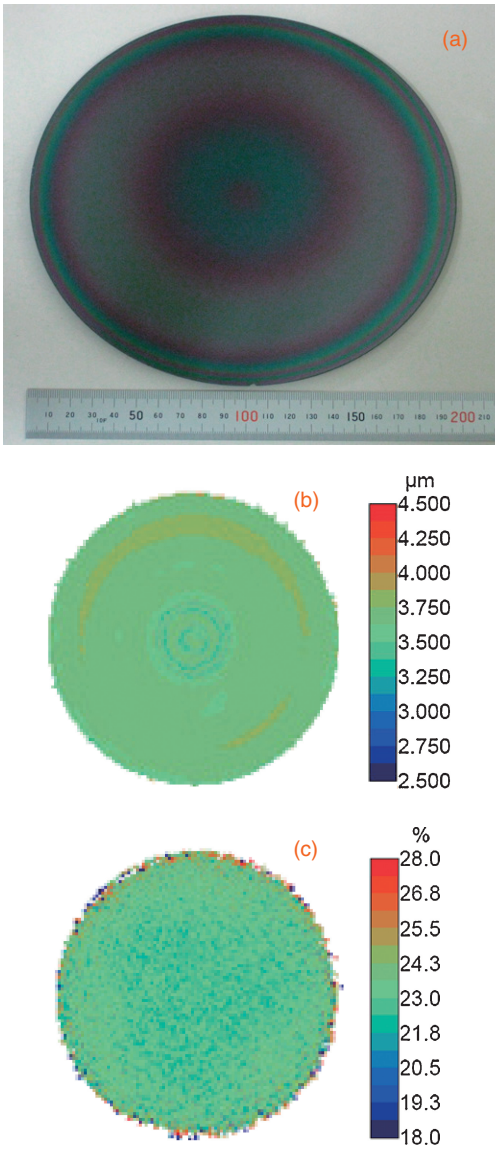

Fig. 1. (a) Image of AlGaN/GaN HEMT grown on a 200-mm-diameter Si(111) substrate. (b, c) Mapping of the epitaxial film thickness and Al composition of AlGaN/GaN carried out by white light interference and photoluminescence, respectively.

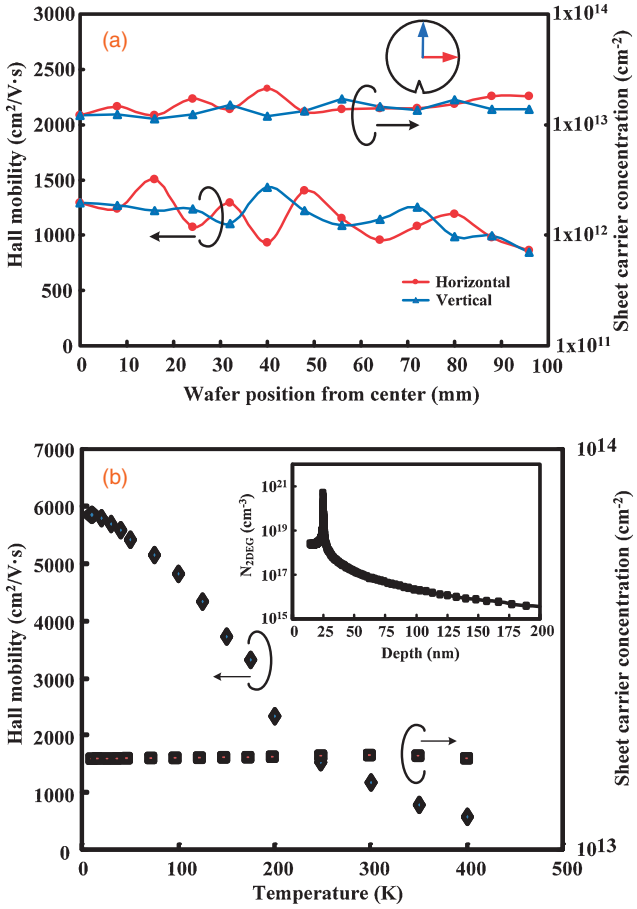

Fig. 2. (a) Variations of Hall mobility and sheet carrier concentration along the horizontal and vertical directions from the center towards the edges of the wafer. (b) Temperature dependence of sheet carrier concentration and Hall mobility of AlGaN/GaN heterostructure. Inset: 2DEG carrier profile in the channel vs depth of epilayers.

superior to that of the epitaxially grown heterostructure reported by Tripathy et al.[9] The wafer bowing of 50 μm is attained for the 3.8-μm-thick epitaxial layer on the 200 mm substrate. This result indicates that the gas phase reaction is minimized in our MOCVD reactor and growth technique.[17,18] The crystalline quality of AlGaN/GaN epitaxial layers was analyzed by high-resolution X-ray diffraction (XRD) measurements. The rocking curves (figure not shown) of (004), (100), and (102) diffraction planes of GaN reveal the full width at half maximum (FWHM) of 478, 1257, and 854 arcsec, the indicative of high-crystalline-quality device grade GaN epitaxy on 200 mm Si. No significant changes in FWHM are observed from the center of wafer to the edges. The estimation of defect densities such as screw and edge dislocations is crucial for the devices to investigate the breakdown mechanism and current collapse phenomena due to charge carrier trapping. The calculated screw and edge dislocation densities for our heterostructure are 4.4×10^8 and $8.0 \times 10^9\,\mathrm{cm}^{-2}$, respectively.

The Hall parameters were extracted from the Van der Pauw method in both horizontal and vertical directions along the radius of the wafer at room temperature as shown in Fig. 2(a). Except the slightly decreasing values of mobility near the wafer edges, the average Hall mobility along both the directions are 1246 and $1225\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, respectively. The maximum Hall mobility as high as 1500 $\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ has been achieved for our MOCVD grown heterostructure. High sheet carrier concentrations of 1.52 and $1.37 \times 10^{13}\,\mathrm{cm}^{-2}$ are obtained from the vertical and horizontal measurements, respectively. Hall mobility and sheet carrier concentrations are uniform throughout the 200 mm wafer, which indicates the substantial improvement in the quality and uniformity of AlGaN/GaN epitaxial layers over large wafer area. Our results on carrier concentration are encouraging compared with the recently reported value of $8.5 \times 10^{12}\,\mathrm{cm}^{-2}$ by Tripathy et al.[9] for a 200 mm Si substrate. On the other hand, the temperature dependence of Hall parameters was studied over the range of temperatures (10 to 300 K) as shown in Fig. 2(b). The increase of Hall mobility over temperature is clearly evident with a room-temperature mobility of $1225\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ and reaches the maximum of $5900\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at 10 K. On the other hand, the sheet carrier concentration is shown to be independent of temperature and remains the same over the range of temperatures. The capacitance–voltage measurement was

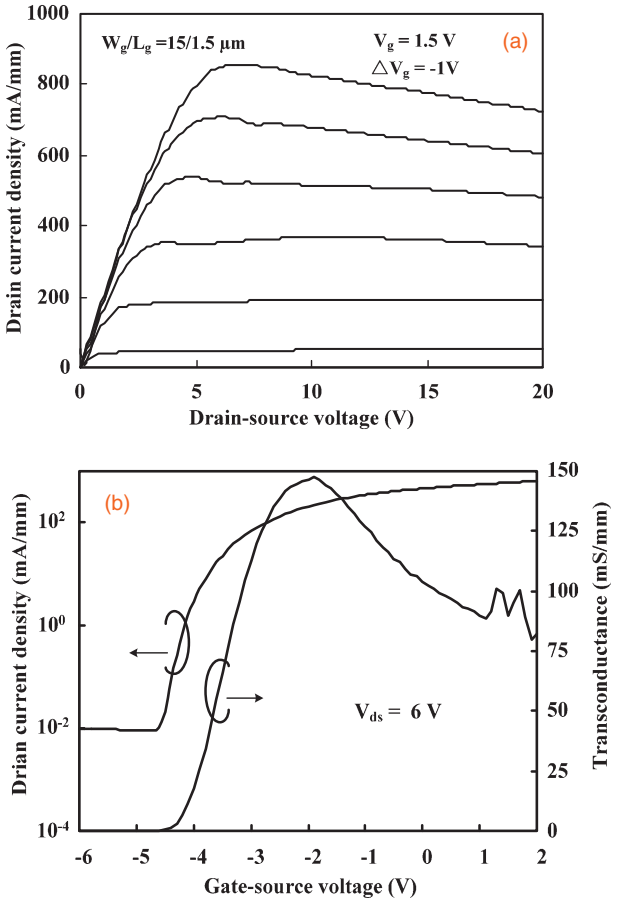

Fig. 3. (a) I–V characteristics and (b) transfer characteristics of AlGaN/GaN heterostructure grown on 200 mm Si substrate.

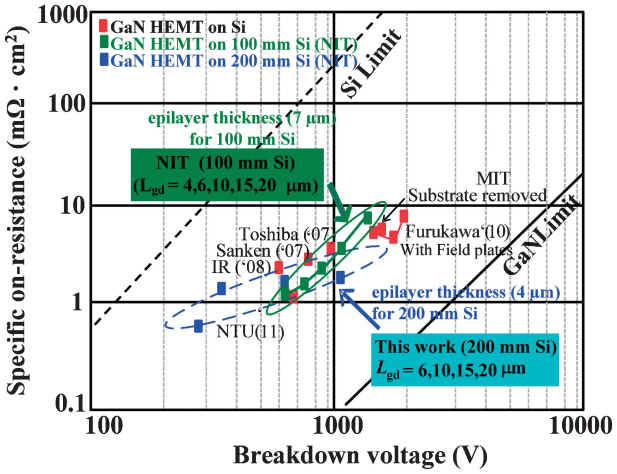

Fig. 4. Specific on-resistance dependence of breakdown voltage for various gate–drain spacing and comparison of results with those of other research groups.

employed at a frequency of 1 MHz, to evaluate the 2DEG concentration versus depth profile as shown in the inset of Fig. 2(b). The evidence for the strong confinement of carriers with the 2DEG carrier concentration of 5.06×10^{20} cm^{-3} located at the depth of 24.8 nm from the AlGaN barrier layers was observed.

Excellent DC characteristics of AlGaN/GaN HEMTs are demonstrated for the device with gate-to-drain distance and gate length of $L_{gd}/L_g = 4/1.5\,\mu m$ using an Agilent B1500A semiconductor parameter analyzer. The maximum drain current density (I_{dsmax}) of 856 mA/mm, the transconductance (g_m) of 153 mS/mm, and the threshold voltage (V_{th}) of −4.2 V obtained are impressive results for the devices fabricated on the 200 mm Si substrate as shown in Figs. 3(a) and 3(b). On the other hand, the drain leakage current is two orders higher than those of conventional AlGaN/GaN HEMT devices fabricated from the 100 mm Si substrate,[12] which we suspect is due to the gate leakage and lateral buffer leakage currents. In order to reduce the gate leakage current, the metal–insulator–semiconductor HEMT (MIS-HEMT) device configuration is effective. Even though the crystalline quality of our GaN epilayers was good, the reason for the lateral buffer leakage current was still unclear. More investigation on the origin of the leakage current may be helpful to understand the breakdown characteristics of our devices. For the lateral leakage measurement, a 20 μm spaced ohmic contacts were biased to a high voltage which exhibited a leakage current of 5.9×10^{-3} mA/mm at 500 V and reaches 0.57 mA/mm around 1 kV. Finally, the permanent device breakdown occurred at 1.1 kV. In order to study the leakage current in buffer along the vertical direction between the ohmic contacts on the surface and at the bottom, a 100-nm-thick Al back ohmic contact was deposited on the substrate.[19] From the current–voltage (I–V) measurements, the flow of leakage current of 9.6×10^{-7} A/cm^2 is recorded and remains constant up to 500 V. On further biasing to 1 kV, the current of 0.23 A/cm^2 is reached, which lead to the breakdown of the device at 1206 V. From these results, the leakage currents in horizontal and vertical directions reveal the fact that the overall structural uniformity of epitaxial layers minimizes the leakage paths and hence improve the device characteristics.

Figure 4 depicts the dependence of specific on-resistance as a function of three-terminal breakdown voltage and its implication on L_{gd} for the HEMT on the 200 mm Si substrate. During breakdown voltage measurement, the devices are immersed in an inert liquid (Fluorinert) to avoid any atmospheric-air ambient surface flash over at the gate–drain region. From the I–V characteristics of $W_g = 200\,\mu m$ devices (at $V_{gs} = 0$ V) R_{ON} was extrapolated for each device for varying L_{gd}. The device on the 200 mm wafer with L_{gd} of 6 μm exhibits R_{ON} of 0.78 mΩ cm^2 which is relatively low compared to our recently reported value[15] of 2 mΩ cm^2 for the same gap length on the 100 mm Si substrate. While on the other hand, a 27% reduction in R_{ON} value i.e., 2.3 mΩ cm^2 for $L_{gd} = 20\,\mu m$ is recorded as compared to 8.5 mΩ cm^2 for the 100 mm substrate. Extensive works on the enhancement of breakdown voltage with low-on-resistance for AlGaN/GaN HEMTs are being reported for 100 mm Si substrates using several techniques including substrate removal and field plates.[16,20] However, these techniques are limited only for small gate–drain distances, where the breakdown voltage is dominated by device geometry.[21] While increasing the thickness of buffer layers on the other hand, eventually improves the quality of the buffer thereby enhancing the breakdown voltage and lowering the on-resistance. Recently, Cheng et al. have reported the two-terminal buffer breakdown voltage of 1380 V with a total buffer thickness of 4.6 μm for the AlGaN/GaN on

200 mm Si.[10] As shown in Fig. 4, we achieved both high 3TBV of 1100 V and low specific on-resistance of 2.3 $m\Omega\,cm^2$ for the HEMT device with a total epilayer thickness of 3.8 µm on the 200 mm Si substrate, which is very much encouraging as compared with the epilayer thickness of 7 µm as reported by our group for devices on the 100 mm Si substrate.[15] Also, the need for the field-plate-like structure is averted to improve the breakdown voltage of the HEMT devices. The power device figure of merit of 5.3×10^8 $V^2\,\Omega^{-1}\,cm^{-2}$ was exhibited by our devices. The demonstration of 3TBV of 1.1 kV with specific on-resistance as low as 2.3 $m\Omega\,cm^2$ and the high FOM for 3.8-µm-thick AlGaN/GaN HEMTs on the 200 mm Si substrate is one of the major steps towards the realization of efficient high-power devices at low cost.

In conclusion, crack-free AlGaN/GaN HEMT epilayers with good surface quality were successfully grown by MOCVD. The heterostructure exhibited high Hall mobility and sheet carrier concentration with a high degree of uniformity over the large substrate area. The high drain current density and transconductance of the devices offered excellent power device characteristics. The demonstration of 1.1 kV off-state 3TBV by the 3.8-µm-thick device with low on-resistance and high figure of merit are the remarkable results revealed by our devices on the 200 mm Si substrate.

Acknowledgment One of the authors would like to thank S. Lawrence Selvaraj (IME, Singapore) for valuable discussion and suggestion on breakdown voltage measurements.

1) X. L. Wang, C. M. Wang, G. X. Hu, J. X. Wang, T. S. Chen, G. Jiao, J. P. Li, Y. P. Zeng, and J. M. Li: Solid-State Electron. **49** (2005) 1387.
2) A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra: Electron. Lett. **40** (2004) 73.
3) M. Higashiwaki, T. Mimura, and T. Matsui: Appl. Phys. Express **1** (2008) 021103.
4) M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo, and K. Joshin: IEDM Tech. Dig., 2005, p. 572.
5) H. Sun, A. R. Alt, H. Benedickter, and C. R. Bolognesi: IEEE Electron Device Lett. **30** (2009) 107.
6) W. S. Tan, M. J. Uren, P. W. Fry, P. A. Houston, R. S. Balmer, and T. Martin: Solid-State Electron. **50** (2006) 511.
7) M. Ishida, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda: Int. Power Electronics Conf., 2010, p. 1014.
8) A. R. Boyd, S. Degroote, M. Leys, F. Schulte, O. Rockenfeller, M. Luenenbuerger, M. Germain, J. Kaeppeler, and M. Heuken: Phys. Status Solidi C **6** (2009) S1045.
9) S. Tripathy, V. K. X. Lin, S. B. Dolmanan, J. P. Y. Tan, R. S. Kajen, L. K. Bera, S. L. Teo, M. Krishna Kumar, S. Arulkumaran, G. I. Ng, S. Vicknesh, S. Todd, W. Z. Wang, G. Q. Lo, H. Li, D. Lee, and S. Han: Appl. Phys. Lett. **101** (2012) 082110.
10) K. Cheng, H. Liang, M. V. Hove, K. Geens, B. D. Jaeger, P. Srivastava, X. Kang, P. Favia, H. Bender, S. Decoutere, J. Dekoster, J. I. D. A. Borniquel, S. W. Jun, and H. Chung: Appl. Phys. Express **5** (2012) 011002.
11) S. Arulkumaran, G. I. Ng, S. Vicknesh, H. Wang, K. S. Ang, J. P. Y. Tan, V. K. Lin, S. Todd, G. Q. Lo, and S. Tripathy: Jpn. J. Appl. Phys. **51** (2012) 111001.
12) S. L. Selvaraj, T. Suzue, and T. Egawa: IEEE Electron Device Lett. **30** (2009) 587.
13) D. Visalli, M. V. Hove, P. Srivastava, J. Derluyn, J. Das, M. Leys, S. Degroote, K. Cheng, M. Germain, and G. Borghs: Appl. Phys. Lett. **97** (2010) 113501.
14) N. Tsurumi, H. Ueno, T. Murata, H. Ishida, Y. Uemoto, T. Ueda, K. Inoue, and T. Tanaka: IEEE Trans. Electron Devices **57** (2010) 980.
15) S. L. Selvaraj, A. Watanabe, A. Wakejima, and T. Egawa: IEEE Electron Device Lett. **33** (2012) 1375.
16) B. Lu and T. Palacios: IEEE Electron Device Lett. **31** (2010) 951.
17) A. Ubukata, K. Ikenaga, N. Akutsu, A. Yamaguchi, K. Matsumoto, T. Yamazaki, and T. Egawa: J. Cryst. Growth **298** (2007) 198.
18) K. Matsumoto and A. Tachibana: J. Cryst. Growth **272** (2004) 360.
19) I. B. Rowena, S. L. Selvaraj, and T. Egawa: IEEE Electron Device Lett. **32** (2011) 1534.
20) W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi: IEEE Trans. Electron Devices **54** (2007) 1825.
21) D. Visalli, M. V. Hove, J. Derluyn, P. Srivastava, D. Marcon, J. Das, M. R. Leys, S. Degroote, K. Cheng, E. Vandenplas, M. Germain, and G. Borghs: IEEE Trans. Electron Devices **57** (2010) 3333.